Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An image processor arranged in operation to generate an interpolated video signal from a received video signal representative of an image, said image processor comprising:

a register store comprising a plurality of register elements and being coupled to[[:]] a control processor,

said register store being arranged in operation to receive said video signal and to provide pixels of said received video signal, under control of said control processor to an interpolator,

selected register elements being connected to said interpolator to provide said pixels of said received video signal for interpolation,

each of said plurality of register elements

being arranged to store a pixel of said received video signal, two or more of said plurality of register elements having ~~and each is~~

an input connected to a first plurality of other register elements and

an output connected to a second plurality of other register elements, and

each of said two or more of said plurality of register elements is

configurable under control of said control processor to feed the pixel stored in said register element to one of said plurality of other

register elements to which said register element is connected in accordance with a temporal reference,

said interpolator being coupled to said register store and arranged in operation to generate said interpolated video signal by interpolating said pixels provided by said register store,

wherein said control processor is operable to detect a feature of said image having both vertical and horizontal components, to control the configuration of said register elements to provide the input pixels associated with said feature to said interpolator to interpolate the feature of said image having both the vertical and the horizontal components.

2. (Canceled)

3. (Previously Presented) The image processor as claimed in Claim 1, wherein said register store comprises a plurality of delay stores coupled in series, a first of the delay stores being arranged to receive said received video signal, each delay store being arranged to delay said received video signal by an amount corresponding to one line of said received video signal, and an output of each of said delay stores is arranged to feed said delayed received video signal to a corresponding register element.

4. (Canceled)

5. (Previously Presented) The image processor as claimed in Claim 3, wherein said plurality of register elements are arranged with reference to a plurality of columns, each column having at least two rows of register elements, the plurality of other register elements to which each of said plurality of register elements is connected being at least two of the register element of the next column, the register element one row above of the next column, and the register element one row below of the next column.

6. (Previously Presented) The image processor as claimed in Claim 5, wherein the pixels stored in each of the plurality of register elements on a substantially diagonal line formed on said column and row arrangement of said plurality of register elements are coupled to said interpolator, the interpolation of the received video signal for the feature having vertical and horizontal components being effected for the pixels stored in the diagonal line of shift registers.

7. (Previously Presented) The image processor as claimed in Claim 1, further comprising:

a clock which is arranged to provide said temporal reference to said register elements, wherein said temporal reference is derived with respect to a rate of receiving said pixels of said received video signal.

8. (Previously Presented) A video camera arranged in operation to produce a video signal representative of an image formed within a field of view of said camera, said video camera having the image processor as claimed in Claim 1 to which said video signal is fed, said image processor being arranged in operation to produce an output video signal by interpolating features of said image having vertical and horizontal components.

9. (Currently Amended) A method of processing an image represented by a received video signal, said method producing an interpolated video signal from said received video signal, said method comprising the steps of:

identifying a feature in said image having a component in both horizontal and vertical dimensions,

identifying the pixels associated with each horizontal line of the video signal,

each of the horizontal lines storing a plurality of said input pixels in a register store,

said register store having a plurality of register elements,

each of said plurality of register elements being arranged to store a pixel of said received video signal, two or more of said plurality of register elements having

an input connected to a first plurality of other register elements and

an output connected to a second plurality of other register elements~~and each of said plurality of register elements being connected to a plurality of other register elements~~, and

generating an output video signal by selectively interpolating said stored plurality of input pixels associated with said feature in accordance with said horizontal and vertical dimensions to generate said interpolated video signal, and

updating said register store in accordance with a temporal reference by feeding the pixel stored in one of said plurality of register elements to one of said plurality of other register elements connected to said register elements.

10. (Original) A computer program providing computer executable instructions, which when loaded onto a computer configures the computer to operate as an image processor as claimed in Claim 1.

11. (Original) A computer program providing computer executable instructions, which when loaded on to a computer causes the computer to perform the method according to Claim 9.

12. (Original) A computer program product having a computer readable medium and having recorded thereon information signals representative of the computer program claimed in Claim 10.